NEC

MOS FIELD EFFECT TRANSISTOR

μPA1763

SWITCHING
DUAL N-CHANNEL POWER MOS FET
INDUSTRIAL USE

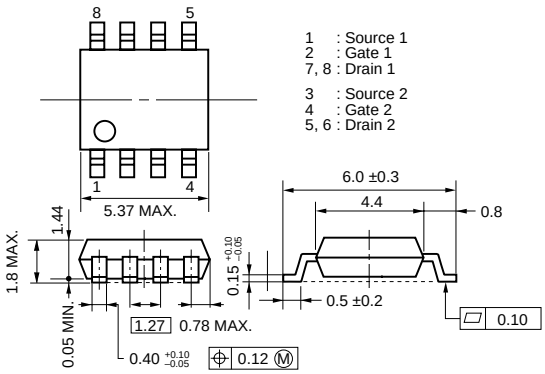
DESCRIPTION

The μPA1763 is N-Channel MOS Field Effect Transistor designed for DC/DC Converters.

FEATURES

- Dual chip type
- Low on-resistance
- ★ $R_{DS(on)1}$ = 47.0 mΩ MAX. (V_{GS} = 10 V, I_D = 2.3 A)
- ★ $R_{DS(on)2}$ = 57.0 mΩ MAX. (V_{GS} = 4.5 V, I_D = 2.3 A)
- ★ $R_{DS(on)3}$ = 66.0 mΩ MAX. (V_{GS} = 4.0 V, I_D = 2.3 A)
- Low input capacitance
- ★ C_{iss} = 870 pF TYP.
- Built-in G-S protection diode
- Small and surface mount package (Power SOP8)

PACKAGE DRAWING (Unit : mm)



ORDERING INFORMATION

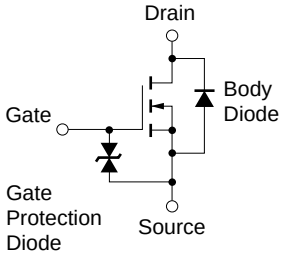
PART NUMBER	PACKAGE
μPA1763G	Power SOP8

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, All terminals are connected.)

	Drain to Source Voltage	V_{DSS}	60	V
	Gate to Source Voltage	V_{GSS}	±20	V
	Drain Current (DC)	$I_{D(DC)}$	±4.5	A
	Drain Current (pulse) Note1	$I_{D(pulse)}$	±18	A
	Total Power Dissipation (1 unit) Note2	P_T	1.7	W
	Total Power Dissipation (2 unit) Note2	P_T	2.0	W
★	Single Avalanche Current Note3	I_{AS}	4.5	A
★	Single Avalanche Energy Note3	E_{AS}	60	mJ
	Channel Temperature	T_{ch}	150	°C
	Storage Temperature	T_{stg}	–55 to + 150	°C

EQUIVALENT CIRCUIT

(1/2 Circuit)



Notes 1. PW ≤ 10 μs, Duty cycle ≤ 1 %

2. T_A = 25 °C, Mounted on ceramic substrate of 1200 mm^2 x 2.2 mm

★ **3.** Starting T_{ch} = 25 °C, R_G = 25 Ω, V_{GS} = 20 V → 0 V

Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage Exceeding the rated voltage may be applied to this device.

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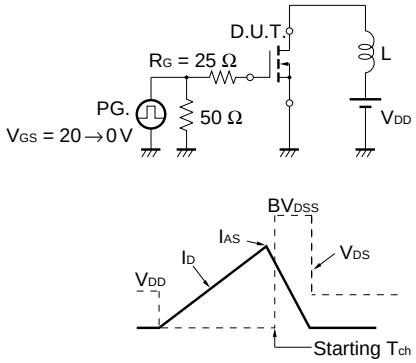
The mark ★ shows major revised points.

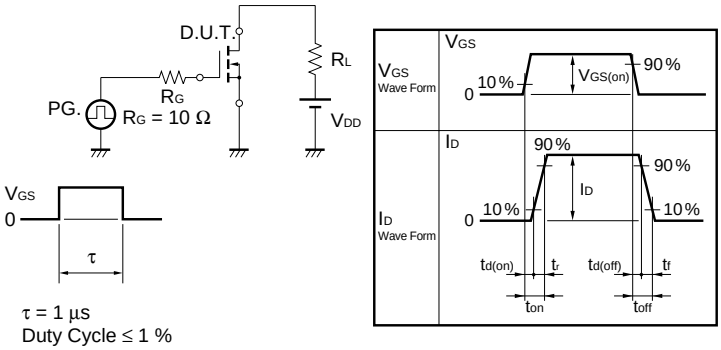
★ ELECTRICAL CHARACTERISTICS (T_A = 25 °C, All terminals are connected.)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	$R_{DS(on)1}$	V_{GS} = 10 V, I_D = 2.3 A		37.0	47.0	mΩ
	$R_{DS(on)2}$	V_{GS} = 4.5 V, I_D = 2.3 A		45.0	57.0	mΩ
	$R_{DS(on)3}$	V_{GS} = 4.0 V, I_D = 2.3 A		49.0	66.0	mΩ
Gate to Source Cut-off Voltage	$V_{GS(off)}$	V_{DS} = 10 V, I_D = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance	$\|y_{fs}\|$	V_{DS} = 10 V, I_D = 2.3 A	3.0	6.0		S
Drain Leakage Current	I_{DSS}	V_{DS} = 60 V, V_{GS} = 0 V			10	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±16 V, V_{DS} = 0 V			±10	μA
Input Capacitance	C_{iss}	V_{DS} = 10 V		870		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		150		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		80		pF
Turn-on Delay Time	$t_{d(on)}$	I_D = 2.3 A		11		ns
Rise Time	t_r	$V_{GS(on)}$ = 10 V		40		ns
Turn-off Delay Time	$t_{d(off)}$	V_{DD} = 30 V		50		ns
Fall Time	t_f	R_G = 10 Ω		12		ns
Total Gate Charge	Q_G	I_D = 4.5 A		20		nC
Gate to Source Charge	Q_{GS}	V_{DD} = 48 V		3		nC
Gate to Drain Charge	Q_{GD}	V_{GS} = 10 V		5		nC
Body Diode Forward Voltage	$V_{F(S-D)}$	I_F = 4.5 A, V_{GS} = 0 V		0.80		V
Reverse Recovery Time	t_{rr}	I_F = 4.5 A, V_{GS} = 0 V		30		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100 A/μs		40		nC

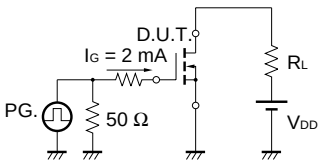
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

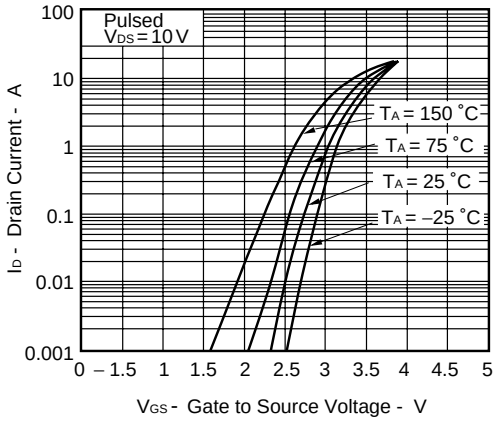


★ **TEST CIRCUIT 3 GATE CHARGE**

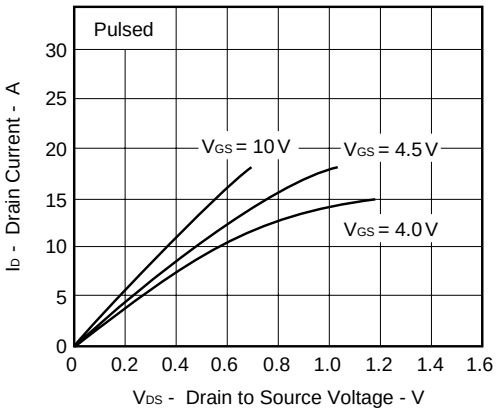


★ TYPICAL CHARACTERISTICS (T_A = 25°C, All terminals are connected.)

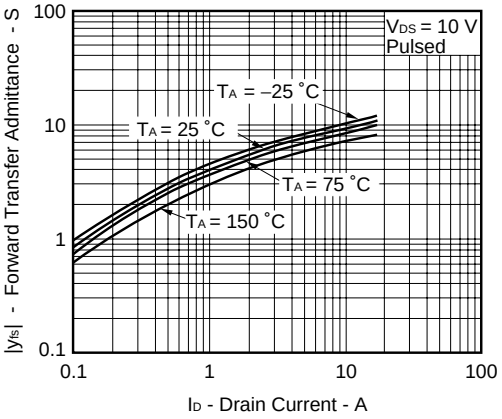
FORWARD TRANSFER CHARACTERISTICS



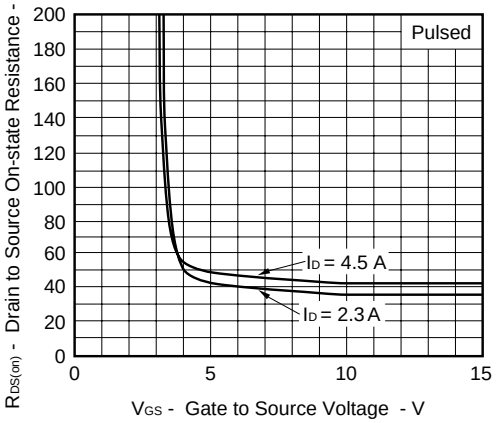
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



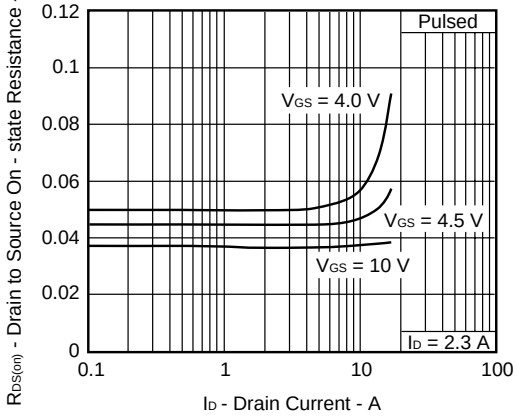
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



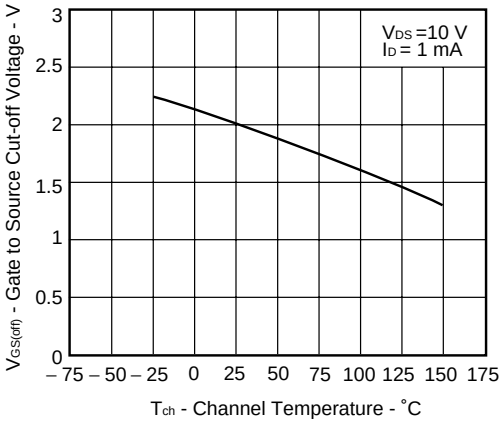
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



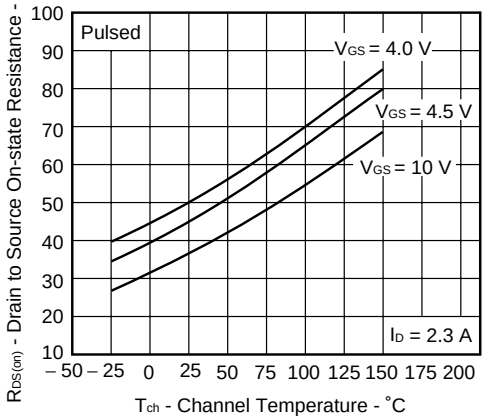
DRAIN TO SOURCE ON-STATE
RESISTANCE vs. DRAIN CURRENT



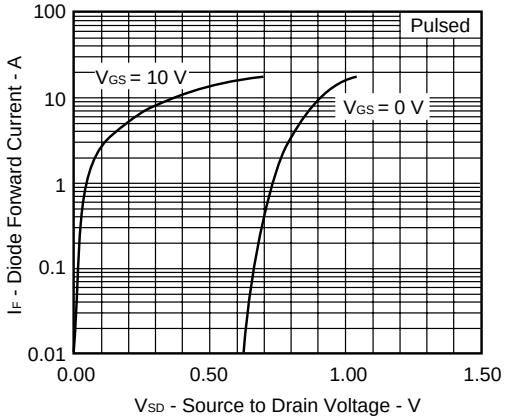
GATE TO SOURCE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE



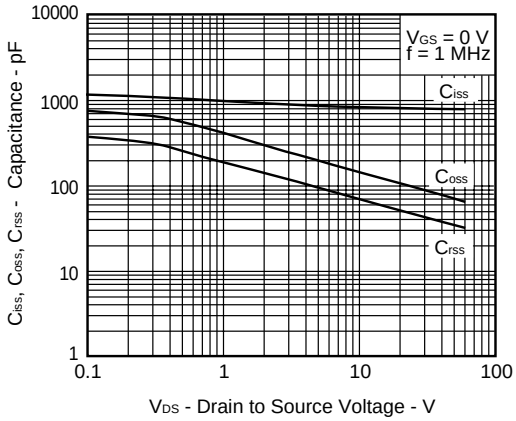
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



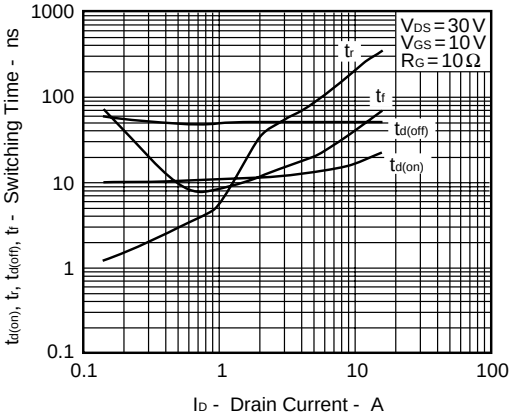
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



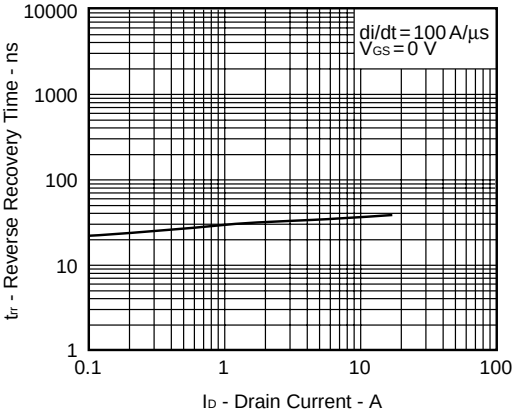
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



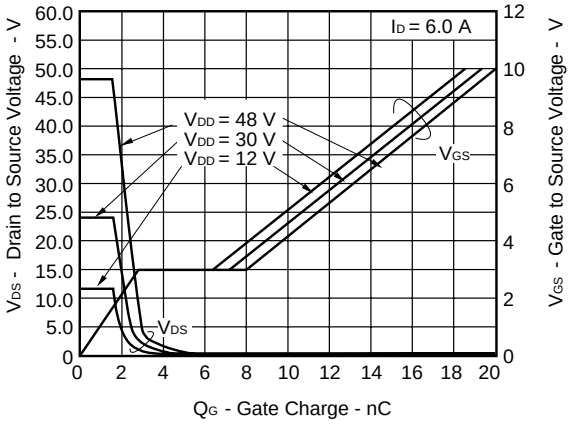
SWITCHING CHARACTERISTICS



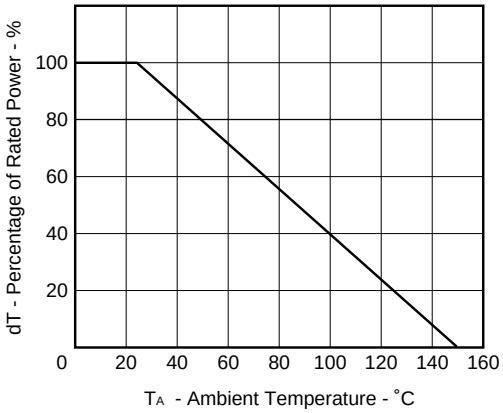
REVERSE RECOVERY TIME vs. DRAIN CURRENT



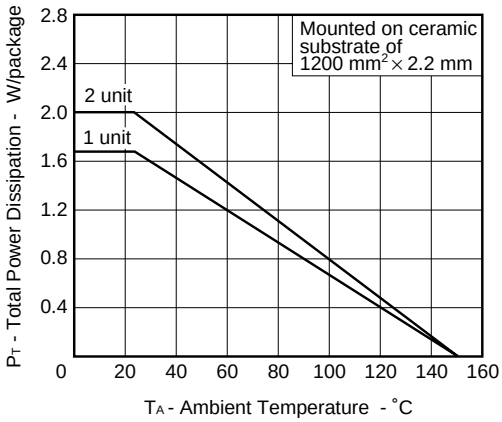
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



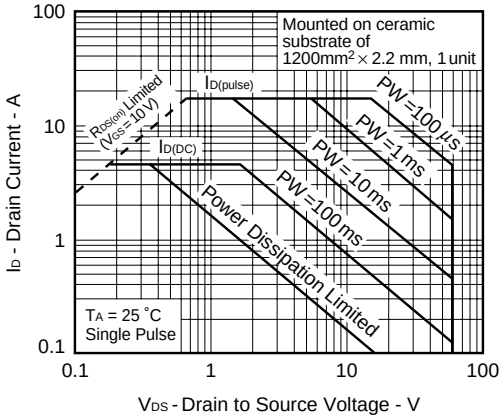
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



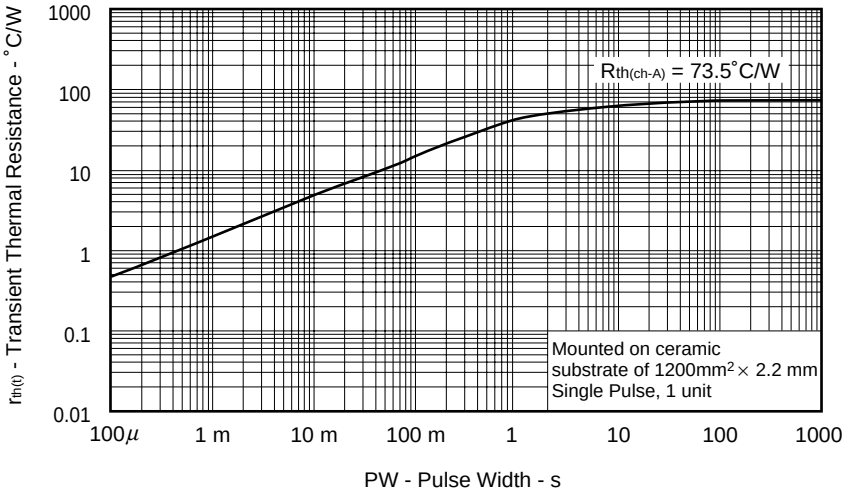
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



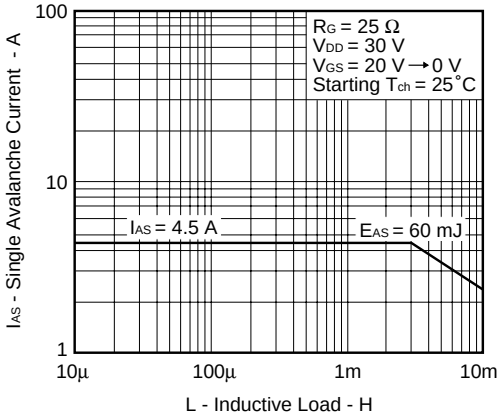
FORWARD BIAS SAFE OPERATING AREA



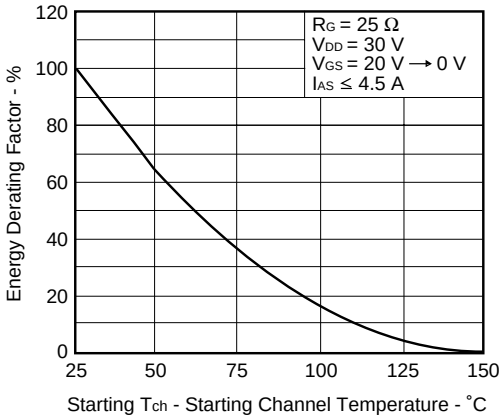
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



SINGLE AVALANCHE CURRENT vs.
INDUCTIVE LOAD



SINGLE AVALANCHE ENERGY
DERATING FACTOR



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